IN THE CLAIMS:

Please cancel claims 3 and 9. **Please also amend** claims 1, 2, 4-8, and 10-12 as shown in the complete list of claims that is presented below.

1. (currently amended) A data processing apparatus comprising:

a CPU configured to operate with one of a plurality of clock frequencies determined in accordance with a selected one of a plurality of clock change signals, a priority order being given to the plurality of clock change signals and the plurality of clock change signals being derived from a plurality of interrupt signals supplied to the CPU;

~~a storage unit for storing plural pieces of CPU operating condition setting information corresponding to the plurality of clock change signals, respectively, the plural pieces of CPU operating condition setting information including at least the plurality of clock frequencies, respectively;~~

a selector for selecting one of the plurality of clock change signals based on the priority order; and

a clock frequency changer for ~~determining the~~ conveying a clock signal having said one of the plurality of clock frequencies to the CPU based on ~~one of the plural pieces of CPU operating condition setting information including~~ the selected one of the plurality of clock change signals.

2. (currently amended) The data processing apparatus according to claim 1 further comprising:

a storage unit for storing plural pieces of CPU operating condition setting information corresponding to the plurality of clock change signals, the plural pieces of CPU operating

condition setting information including a plurality of memory access timings corresponding to the plurality of clock change signals; and

a detector for determining whether a memory access is currently being performed, ~~and~~

wherein ~~the plural pieces of CPU operating condition setting information include a plurality of memory access timings corresponding to the plurality of clock change signals, and~~ the clock frequency changer is inoperative when the detector determines that ~~the~~ a memory access is currently being performed, and

wherein the clock frequency changer conveys the clock signal having said ~~determines~~ ~~the~~ one of the plurality of clock frequencies together with CPU operating condition setting information having one of the plurality of memory access timings based on the selected one of the plurality of clock change signals ~~plural pieces of CPU operating condition setting information~~ when the detector determines that ~~the~~ a memory access is not currently ~~unperformed.~~ being performed.

Claim 3 (cancelled).

4. (currently amended) The data processing apparatus according to claim 2, wherein the plurality of clock change signals correspond to a plurality of interrupt signals provided to the ~~CPU, respectively.~~ CPU.

5. (currently amended) The data processing apparatus according to claim 1, wherein the priority order is decided in accordance with a value of a clock frequency. ~~determined in connection with each of the plurality of clock change signals.~~

6. (currently amended) The data processing apparatus according to claim 1 further comprising a clock stop unit for preventing passage of ~~a~~ the clock signal to the CPU, and a stop cancellation unit for resuming the passage of the clock signal to the CPU in response to at least one of the plurality of clock change signals.

7. (currently amended) A data processing apparatus comprising:

a CPU configured to operate with one of a plurality of clock frequencies determined in accordance with a selected one of a plurality of clock change signals, a priority order being given to the plurality of clock change signals and the plurality of clock change signals being derived from a plurality of interrupt signals supplied to the CPU;

~~storage means for storing plural pieces of CPU operating condition setting information corresponding to the plurality of clock change signals, respectively, the plural pieces of CPU operating condition setting information including at least the plurality of clock frequencies, respectively;~~

selecting means for selecting one of the plurality of clock change signals based on the priority order; and

clock frequency changing means for ~~determining the~~ conveying a clock signal having said one of the plurality of clock frequencies to the CPU based on ~~one of the plural pieces of CPU operating condition setting information including~~ the selected one of the plurality of clock change signals.

8. (currently amended) The data processing apparatus according to claim 7 further comprising:

storage means for storing plural pieces of CPU operating condition setting information corresponding to the plurality of clock change signals, the plural pieces of CPU operating condition setting information including a plurality of memory access timings corresponding to the plurality of clock change signals; and

~~a~~ detecting means for determining whether a memory access is currently being performed, ~~and~~

wherein ~~the plural pieces of CPU operating condition setting information include a plurality of memory access timings corresponding to the plurality of clock change signals, and~~ the clock frequency changing means is inoperative when the detecting means determines that ~~the~~ a memory access is currently being performed, and

wherein the clock frequency changing means conveys the clock signal having said ~~determines the one~~ of the plurality of clock frequencies together with CPU operating condition setting information having one of the plurality of memory access timings based on the selected one of the plurality of clock change signals ~~plural pieces of CPU operating condition setting information~~ when the detecting means determines that ~~the~~ a memory access is not currently ~~unperformed.~~ being performed.

Claim 9 (cancelled).

10. (currently amended) The data processing apparatus according to claim 8, wherein the plurality of clock change signals correspond to a plurality of interrupt signals provided to the ~~CPU, respectively.~~ CPU.

11. (currently amended) The data processing apparatus according to claim 7, wherein the priority order is decided in accordance with a value of a clock frequency. ~~determined in connection with each of the plurality of clock change signals.~~

12. (currently amended) The data processing apparatus according to claim 7 further comprising a clock stop means for preventing passage of ~~a~~ the clock signal to the CPU, and a cancellation means for resuming the passage of the clock signal to the CPU in response to at least one of the plurality of clock change signals.